**Review questions chapter 3**

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| **1.** **What general categories of functions are specified by computer instructions?**  The categories are processor-memory, processor-I/O, data processing, and c ontrol.  **2.** **List and briefly define the possible states that define an instruction execution**.   * **Instruction address calculation** (iac): Determine the address of the next instruction to be executed. * **Instruction fetch** (if): Read instruction from its memory location into the processor. * **Instruction operation decoding**: Analyze instruction to determine type of operation to be performed and operand(s) to be used. * **Operand address calculation** (oac): If the operation involves reference to an operand in memory or available via I/O, then determine the address of the operand. * **Operand fetch** (of):  Fetch the operand from memory or read it in from I/O. * **Data operation**:  Perform the operation indicated in the instruction. * **Operand store** (os):  Write the result into memory or out to I/O.   **3. List and briefly define two approaches to dealing with multiple interrupts**.  **Disabling interrupts**- processor has the ability to and will ignore the specific interrupts. Those interrupts remain pending and will be checked after the processor has enabled interrupts.  **Interrupt service routine(ISR)** - priorities assigned to the different types of interrupts. Interrupt service routines with higher priorities can interrupt ones with lower priority, in which case the ISR with the lower priority is put on the stack until that ISR is completed.  **4. What types of transfers must a computer's interconnection structure (e.g. bus) support?**  Memory to processor, processor to memory, I/O to processor, processor to I/O, and I/O to or from memory.  **5. What is the benefit of using a multiple-bus architecture compared to a single-bus architecture?**  It is efficient, since if only one bus is for everything, only one device can then communicate at a time, since if more than one device were to try and send data on the single bus, transmission would be garbled. |